PHOTOMASK

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Demonstration of full field patterning of 32 nm test chips using EUVL

Gilroy Vandentop, Manish Chandhok, Ernisse S. Putna, Todd R. Younkin, James S. Clarke, and Steven Carson, Intel Corporation, Hillsboro, OR 97124

Alan Myers and Michael Leeson, Intel Corporation, IMEC (Belgium)

Guojing Zhang and Ted Liang, Intel Corporation, Santa Clara, CA 95054

Tetsunori Murachi, Intel K.K., Tsukuba-shi, Ibaraki-ken, Japan

ABSTRACT

EUV lithography is considered one of the options for high volume manufacturing (HVM) of 16 nm MPU node devices.[1] The benefits of high k_1(~0.5) imaging enable EUVL to simplify the patterning process and ease design rule restrictions. However, EUVL with its unique imaging process – reflective optics and masks, vacuum operation, and lack of pellicle, has several challenges to overcome before being qualified for production. Thus, it is important to demonstrate the capability to integrate EUVL into existing process flows and characterize issues which could hamper yield. A patterning demonstration of Intel's 32 nm test chips using the ADT at IMEC[7] is presented, This test chip was manufactured using processes initially developed with the Intel MET[2-4] as well as masks made by Intel's mask shop.[5,6] The 32 nm node test chips which had a pitch of 112.5 nm at the trench layer, were patterned on the ADT which resulted in a large k_1 factor of 1 and consequently, the trench process window was iso-focal with MEEF = 1. It was found that all mask defects detected by a mask pattern inspection tool printed on the wafer and that 90% of these originated from the substrate. We concluded that improvements are needed in mask defects, photospeed of the resist, overlay, and tool throughput of the tool to get better results to enable us to ultimately examine yield.

1. Introduction

EUVL is slated to be in production for the 16 nm node, however, the technology has several hurdles to cross before being considered for development let alone manufacturing. The technology cycle at Intel starts several years before production begins. We first start with

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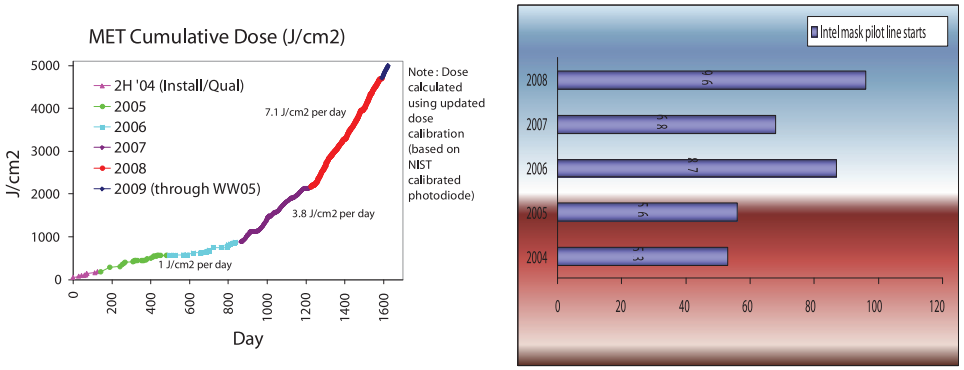

Figure 1. The number of shots logged on the MET (left) shows high productivity in 2008. The number of mask pilot line starts (right) has increased since 2004 with close to 100 starts this year.

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TAKE A LOOK INSIDE:

EDITORIAL

The Future of the photomask industry.

Emmanuel Rausa, Plasma-Therm LLC

The severe downturn in the economy is having an impact at every level in our industry. It accelerates the consolidation rates and refocuses importance of the low cost no thrill mask operations at the expense of more advanced operations. However, other than maybe postponing it, it is probably too late to truly affect the 22nm node technical solution.

It is fairly clear for most advanced chip manufacturers what the lithography solution will be for the 22nm node. If we had to compare this to noise cancelling headphones, I would say most fabs have the electronics, the headphones, but the power management might be an issue (finding a pair of new batteries in the middle of the flight is almost impossible) and it is almost guaranteed that the cost will be on the high side. It may be not the most elegant assembly solution but brute force and time will get us there.

What about 16nm? There are two possible outcomes that I think are out of our control.

First, this economic crisis is not so deep as to radically affect behaviors. By the time we arrive at the 16nm cycle introduction, the current down turn could be seen or remembered as one further cycle in a business that is familiar with booms and busts, or to be more in line with the other current actuality, no bigger than what the Swine flu scare turned out to be today. Conclusion: everyone is quite happy to pursue technology improvement for maximized economic performance, but it is likely be a gradual improvement over what exists today.

Second option, the crisis is so deep that it will take 10 to 15 years before, on average the most advanced economies come back to a 2007 level. Say we are facing not the Swine (AH1N1) flu but the 1918 Spanish influenza when over 50 million people caught the virus, started bleeding (as in blood not cash) through nose and eyes and were dead in as little as two days. A simple technology/cost advantage will not do as the whole infrastructure would also change. The solution in that case will be so different that I would argue it is currently not on the roadmap and people will need to truly think out of the box. I cannot assess the depth of the economic problems, or what technology will be used for 16nm. I am however confident that brilliant scientists and engineers will be delivering a solution with the parameters and constraints put around them. Progress will not stop, but how we view and judge progress may indeed change.

So let's go back on the noise cancelling head phones comparison for a minute. Say I was willing to pay $450 for the top of the line equipment in a smallish down turn. Under a major recession with no end in sight, one would ask do I need all the expense of the brand recognition and the digital signal processing, etc. For all intended purposes, as a colleague of mine was pointing out recently, I can use the regular in-ear headphone provided by the airline, and put on construction worker industry standard ear muff protection. I have the correct sound and good noise cancelling (20 to 25dB) for a total of about $20!

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Managing Editor/Graphics Linda DeLano
Advertising Teresa Roles-Meier
BACUS Technical Group Manager Pat Wight

SPIE

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290 or +1 888 504 8171
Fax: +1 360 647 1445
SPIE.org
customerservice@spie.org

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Table 1. Comparison of EUV exposure tools: Intel MET, Nikon EUV1, and ASML ADT.

	Intel MET	Nikon EUV1	ASML ADT
Field size	(600 x 600) μm^2	(26 x 33) mm^2	(26 x 33) mm^2
NA	0.3*	0.25	0.25
Illumination	0.36/0.55 annular	0.5-0.8 disk + OAI	0.5 disk
Flare	~7%	~12%	~16%
Overlay	No	Yes	Yes

* 10% by area central obscuration

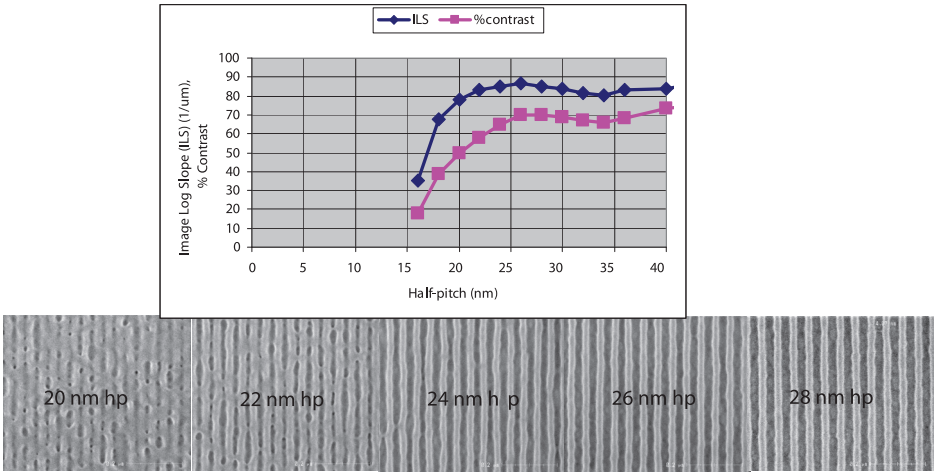

Figure 2. Aerial image prediction of the aerial image log slope and contrast Vs half pitch for the Intel MET (above). SEM of sub 30 nm hp nested features (below). LWR of 3.5-4 nm is observed for hp up to 26 nm hp; below that pattern collapse and aerial image resolution loss dominate.

research to understand the key limiters to the technology and look at several options. The research phase can be several years long depending on the complexity and resources. If the technical barriers in the research phase are overcome, then the technology goes into the pathfinding (PF) stage. The PF stage typically lasts about 2 years during which we establish baseline process capability and support design rule explorations.

The last phase before we ramp into manufacturing is the most crucial phase which we call technology development. Technology development (TD) is where we integrate the new technology with the rest of the chip making process to get high yielding test chips. TD can last anywhere from 11/2 to 2 years and requires the infrastructure needed to support HVM be in place.

At Intel, we have been involved in EUV lithography research for many years and have been at the forefront of improving photoresist performance using the Intel MET.[2] We have a committed engagement with photoresist suppliers, universities, and research institutes which resulted in over 250 resists being screened on the MET just the last year alone. The photoresist development has been enabled by the high uptime of the Intel MET as seen in the increasing number of shots put on the MET over the past 5 years (Figure 1). Intel has had a fully functioning EUV mask pilot line since 2004.[5,6] The number of starts in the mask pilot line has been increasing steadily over the years and this year we are on track to start over 100 masks (Figure 1). These activities in the area of EUV tools, mask, resists as well as other technologies, have gone a long way in enabling EUV lithography.

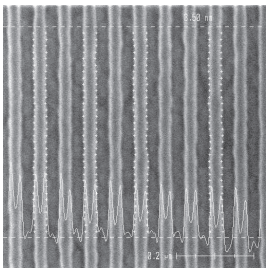

Figure 3. 32 nm hp lines/ spaces imaged with the ADT at IMEC. LWR is 3.5 nm.

Process development at Intel has been limited to "circuit level" lithography and etch due to the small field size of the MET. For full-chip integrated process development, a full-field tool is required. Two such tools are now available to Intel: ASML's ADT, and Nikon's EUV1. A comparison of the main features of the MET, ADT, and EUV1 is outlined in Table 1.

The MET has a small field but low flare and good imaging down to 26 nm half-pitch (hp) (Figure 2). The Alpha Demo Tool (ADT) at IMEC is a full field EUV lithography tool having a NA of 0.25, fixed σ of 0.5, and flare of ~16%. Despite the high flare of the ADT, 32 nm hp patterns can be resolved with reasonably low LWR of 3.5 nm (Figure 3) using the same photoresist process developed on the Intel MET (as shown in Figure 2).

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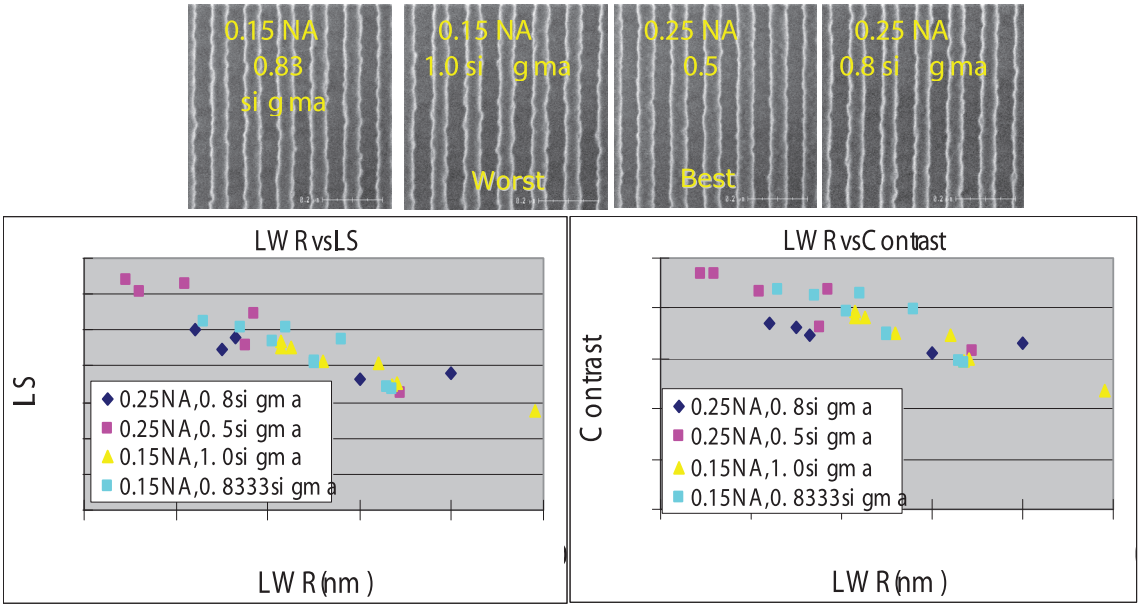

Figure 4. Data from EUV1 showing that LWR is inversely proportional to ILS and Contrast by modulating the aerial image using different combinations of NA and partial coherence (sigma). The best imaging is seen for 0.25 NA, 0.5 sigma and the worst imaging is for 0.15 NA and sigma of 1.

Table 2. Pitches used in Intel's 32 nm high performance logic technology test chips.

Layer	Pitch (nm)
Isolation	140.0
Contacted gate pitch	112.5
Metal 1-3	112.5
Metal 4	168.8
Metal 5	225
Metal 6	337.6
Metal 7	450.1

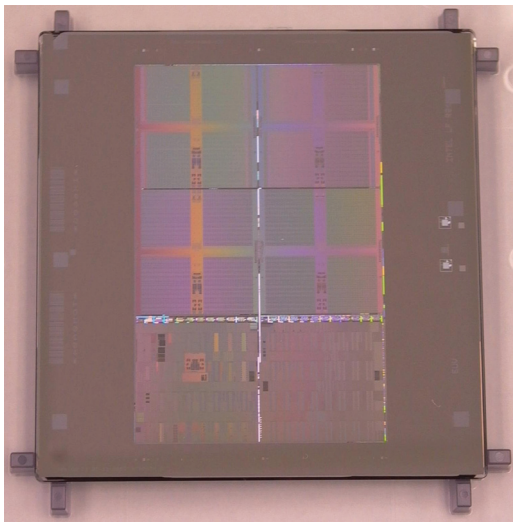

Figure 5. Full field EUV mask used for patterning 32 nm test chips.

Even with a low throughput of ~1-2 wafers/hour, the overlay capability of the ADT tool allows us to print our full-field test chips.

The other full-field tool available to Intel is Nikon's EUV1 tool. EUV1 has an NA of 0.25, flare of ~12%, overlay capability, and partial coherence flexibility as well as off-axis illumination. EUV1 has the exchangeable NA stops for 0.15 or 0.25 NA as well as exchangeable sigma aperture stops. The EUV1 tool has sigma as high as 0.8 for 0.25 NA and sigma of 1 for NA of 0.15. Using these illumination combinations, we observe trends in aerial image log slope (ILS) and contrast which are inversely proportional to Line Width Roughness (LWR): higher ILS/contrast results in lower LWR and vice versa (Figure 4). Flexibility of illumination conditions will be valuable for sub-30nm hp process development.

Currently, Intel is completing the final phase of its 32 nm technology node process development which uses immersion lithography for patterning the critical layers. Details of the transistor performance are described[8] and the replacement metal gate (RMG) process flow.[9] Table 2 summarizes key design rules for the 32nm logic node.[8] 112.5 nm is the most aggressive contacted gate pitch reported for 32nm high-performance logic technologies. In this paper we will present the results of integrating one of the critical layers, for patterning our 32 nm test chips using EUVL on the ADT at IMEC.

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Table 3. Summary of particle adders measured on EUV blanks for particles ≥ 100 nm based on 100% capture over an inspection area = (142 x 142) mm².

Process	Average adders/pass
Shipping	~7
Transfer to reticle box	~4
Exposure tool load/clamp/unclamp/unload	~1

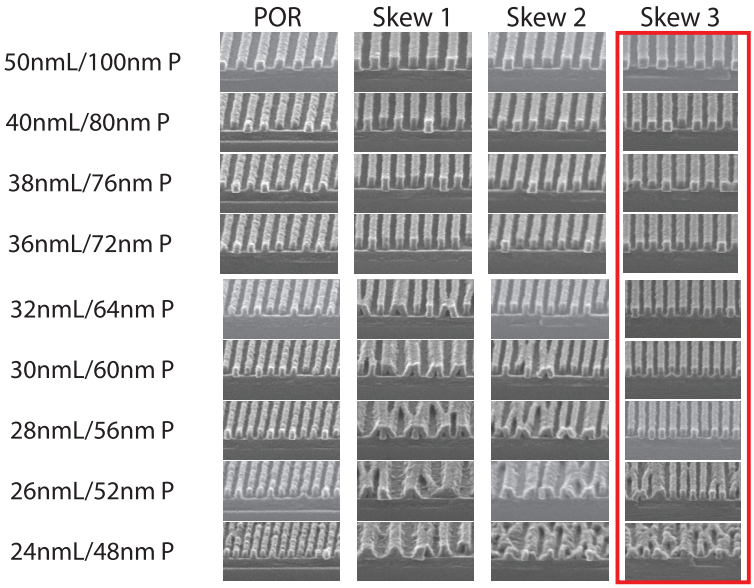

Figure 6. Cross-section profiles of the photoresist used for trench patterning as a function of different bake skews. Skew 3 shows nice vertical profiles down to 28 nm hp; below 28 nm hp this photoresist exhibits pattern collapse.

2. Reticle Manufacturing and Adders from Reticle Handling

The mask pilot line at Intel, besides the standard mask making tools, has also incorporates a complete set of tools to characterize EUV masks including blank inspection, non-flatness measurements, EUV reflectivity measurements, absorber film stack film deposition, and mask cleans. For the ADT, our masks use a low thermal expansion material (LTEM) substrate. The multi-layer (ML) stack consists of 40 Mo-Si bi-layers capped by 2.5 nm of Ru. The absorber consists of 87 nm thick TaN-TaON film stack. For e-chucking, the backside (BS) of the mask has a 70 nm thick CrN conducting film. The peak EUV reflectivity measured at 13.56 nm was 63.9% in the clear (ML) region and 0.6% in the absorber. The test chip pattern covers the full scan length (33 mm at 1X) of the exposure tool (Figure 5).

After mask patterning, the mask was inspected and shipped to IMEC. At IMEC the mask was manually transferred into a special reticle box in a Class 1 clean room to minimize particle adders. The reticle box is then loaded into the ADT. Due to the lack of a pellicle, one of the concerns for EUV lithography is that particles will be added to the pattern side of the reticle inside the exposure tool as well as during its shipping and handling. Segmented studies on the particle adders to EUV mask blanks were collected. Pre and post scans quality area of 142x142 mm² were measured with Intel's Lasertec M1350 which has 100% capture rate of particles ≥ 100 nm. In the exposure tool, 50 cycles of load/unload on the ADT with clamping onto the reticle chuck were run to obtain the average number of adders per cycle. Table 3 summarizes the particle adder data which shows that on an average, ~7 particles are added during shipping, ~ 4 particles added during the transfer into the reticle storage box, and about 1 particle was added during one cycle of the load/clamp/unclamp/unload process inside the exposure tool. Even though just 1 particle was added in the exposure tool/cycle, eventually, after several load and unloads the reticle will have too many defects and will need to be cleaned. We have determined that all the particle adders in our blank tests can be cleaned using standard wet chemistries. However, it would be better to have a large reticle storage library under vacuum in the exposure tool to minimize the need for multiple loads and unloads.

3. Trench Process

While we are developing several front end processes at Intel using the MET, for the 32 nm test chip demonstration using

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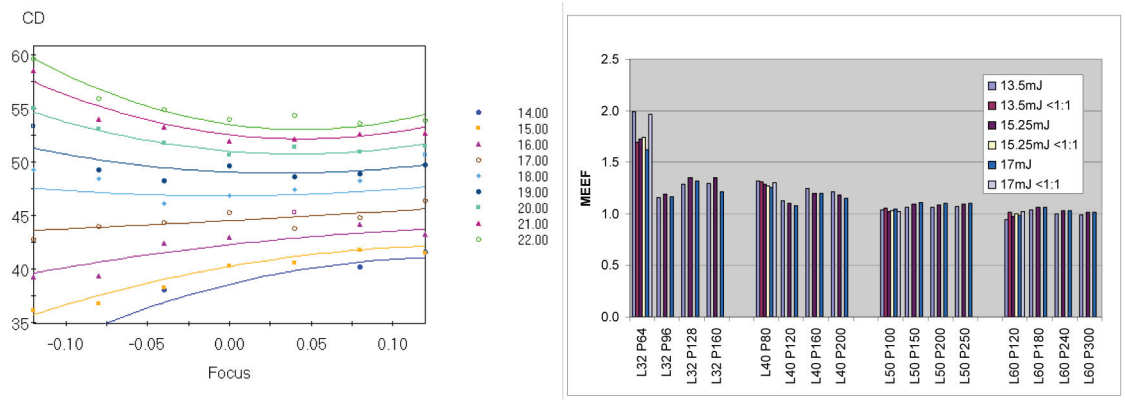

Figure 7. Bossung curve (CD through focus and dose) for 45 nm drawn CD trenches, 116 nm pitch (left). MEEF's of the trenches as a function of CD and pitch.

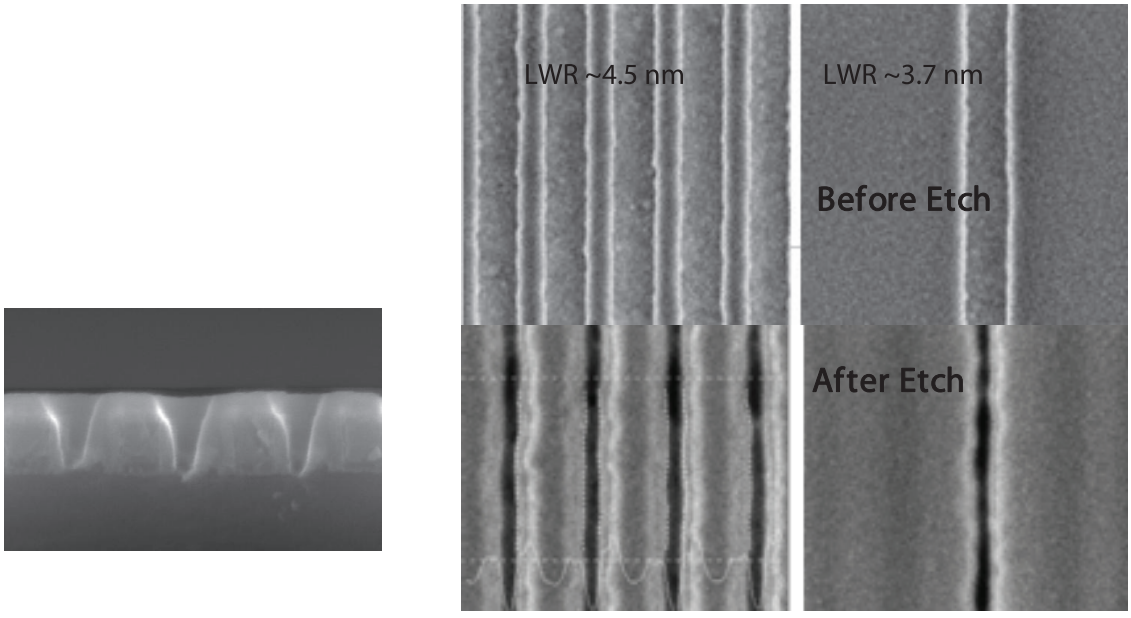

Figure 8. Top down SEMs of nested and isolated trenches before (above) and after etch (below). Cross-section of nested trenches after etch and cleans is shown on the left.

EUVL, due to the high flare of the ADT, we selected a dark field trench pattern. The expected flare based on convolution of the point spread function due to scatter (PSF_{sc}) of the ADT and the mask pattern is <2%. The photoresist process (60 nm resist thickness) was optimized by modifying the bakes and thickness on the Intel MET to give near vertical sidewall angle for half-pitches down to 28 nm hp. It was found that below 28 nm hp, this resist exhibits pattern collapse (Figure 6). The optimized process recipe was then transferred to IMEC.

Using the ADT, 45 nm trenches at 116 nm pitch at a dose of 17 mJ/cm^2 have a depth of focus (DOF) greater than 0.25 µm and appears iso-focal (Figure 7). The high exposure dose resulted in a low throughput of ~1 wafer/hour. The measured mask error enhancement factor (MEEF) is nearly 1 for all features that are at pitches of 100 nm and above (Figure 7). In fact even down 80 nm pitch, the MEEF is less than 1.5. Due to the relatively high k1 of ~1 for the pitch of 112.5 nm in the 32 nm test chip, minimal optical proximity correction (OPC) was required. Rule based OPC was applied to bias the CD to compensate for etch. Photoresist acid diffusion caused corner rounding and trench end pullback was compensated for through the use of hammerheads.

The trenches patterned using EUV have relatively low LWR of 4-5 nm (3 σ) (Figure 8). The etch process has a large negative bias but it had no issues clearing all the way to the bottom of the trench as can be seen in the cross-section SEM in Figure 8. Etch process optimization is needed for the film stack with the EUV resist.

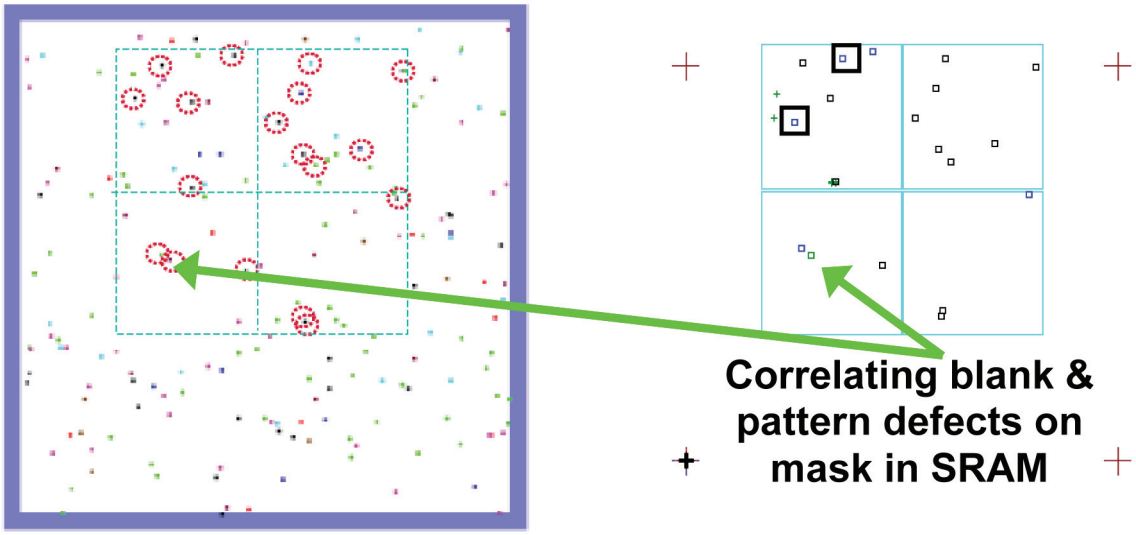

Figure 9. Several defects were found on the blank (left) that were picked up by die-die comparison in the SRAM region after mask patterning (right). In the pattern inspection map (right), absorber defects are highlighted by large black squares. The remaining marks are blank defects whose locations are circled in the blank inspection data (left).

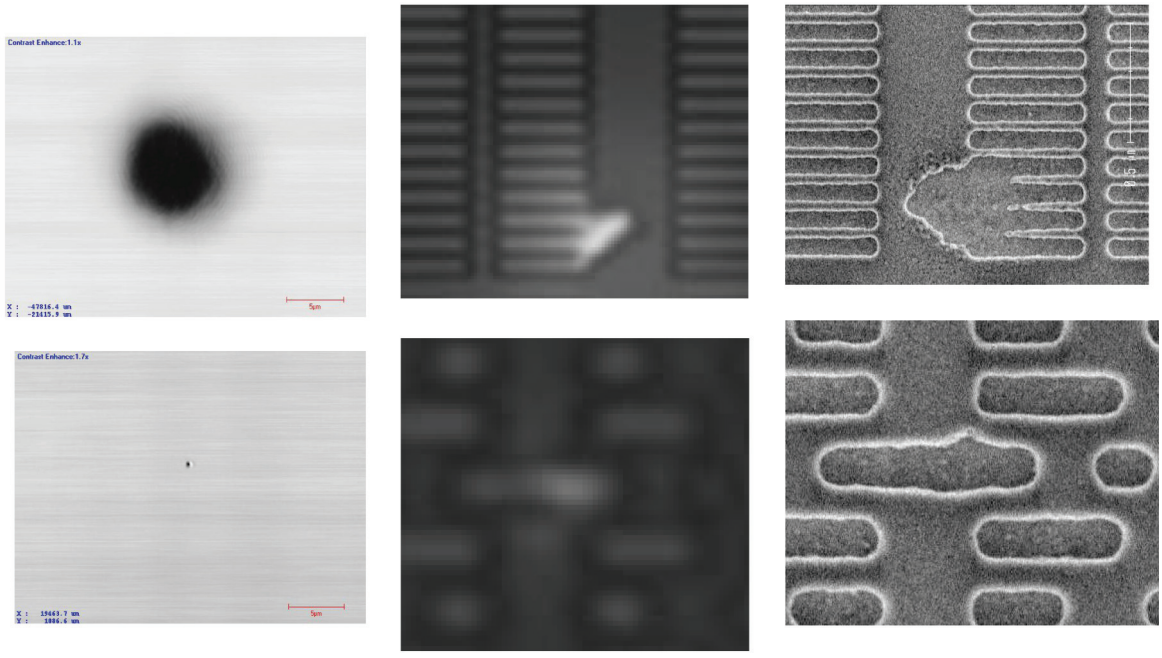

Figure 10. Sample images of the 2 defects as imaged by the blank inspection tool (left), the mask pattern inspection tool (center), and the SEM of the wafer (right). The size of the smaller ML defect above is about 100nm based on M1350 pixel size. The mask pattern inspection image and wafer print image are a mirrored due to the reflective mask used for EUV.

4. Deefect Printability

Prior to deposition of the absorber, the blank was inspected using a Lasertec M-1350 inspection tool, where several defects were detected (Figure 9, left). The bulk of the substrate defects were pits created during the substrate polishing process. After the absorber was patterned, the mask was inspected on a mask pattern inspection tool. Inspection of this mask was done at low sensitivity (>> 70 nm, the POR sensitivity). Using the die-die inspection capability in the SRAM region (Figure 9, right), 19 defects were captured, of which 17 were correlated to blank defects (circled in the blank defect data map

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in Figure 9, left). Due to the reduced sensitivity, only 2 large pattern (absorber) defects were found, the locations of which are highlighted by large squares in the mask pattern defect map (Figure 9, right). Inspection of the exposed wafers was done to determine defect printability. All 19 defects detected at mask inspection were printable.

In Figure 10, two of the blank defects that impacted patterns in the SRAM area are shown as imaged by the blank inspection tool, mask pattern inspection tool, and SEM on wafer, respectively. These blank defects are > 100 nm (4X). The mask pattern inspection image and wafer print image are mirrored due to the reflective mask used for EUV.

5. Future Work

For this 32 nm test chip demonstration, mix and match overlay between EUV and 193 nm lithography was not as good as pure 193 nm, which is limiting our ability to obtain e-test data off the EUV patterned test chips. Once the overlay has improved, e-test data will be collected for resistivity, I_{on} Vs I_{off}, as well as single cell SRAM functionality. Further process development will also be done where multiple layers patterned using EUV are integrated, as well as fabricating 22 and 16 nm test chips. Defectivity caused by particles added due to the lack of a pellicle will be characterized on patterned wafers to characterize their impact on yield.

6. Summary

Steps towards integration of a single trench layer patterned using EUVL into Intel's 32 nm process has been demonstrated. Due to the high k_1(~1) at 112.5 nm pitch with the ADT, DOF is > 250 nm, and MEEF ~1, requiring minimal OPC. There were no issues in matching the final trench targets after etch to Intel's standard 32 nm process. Some of the improvements required in the exposure tool include mix-match overlay and throughput. Photoresist photospeed could be faster to enable better throughput. All the defects detected on the mask at reduced sensitivity using the mask pattern inspection tool were printed on the wafer. Reduction of ML defects, particularly due to pits, is necessary to obtain yielding test chips.

7. Acknowledgments

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Industry Briefs

It's EUV Again: Two Recent Viewpoints

IMEC sees 22nm EUV SRAMs as call to action. Extending work with EUV and SRAMs from last summer's 32nm achievement, IMEC now says it has developed the "world's first" functional 22nm CMOS SRAM cells made using EUV lithography, including the first metal layer.

Results presented at SEMICON West 2008 only used EUV to print the contact holes in 32nm SRAMs; now IMEC used an ASML EUV alpha tool to pattern both the contact (~45nm size) and metal-1 layer (60nm width, 46nm spaces). Overlay performance is "good," IMEC said, adding that a single-patterning approach "further strengthens the case for EUV as a cost-effective solution." The cells, made with FinFETs, have a density of 0.099 um2, 47% smaller than the 32nm cell reported last year. FinFET layers were printed using ASML's 1900i immersion litho tools.

Resolution has improved from 35-40nm down to 25-30nm in the past six months, and line-edge roughness (LER) has moved from 5-6nm down to 4nm, with resist sensitivities of around 15-20mJ/cm^2. The goal of 22nm resolution will require more development in optics toward higher NA and off-axis illumination (capabilities not present on the current ASML alpha tool), but which they promise will be in the preproduction tools due in 2010. Target resist sensitivity of 10mJ/cm^2 "seems achievable in time," IMEC added.

Two big sticking points for EUV development still need work: optics and resists. For optics, Zeiss is working "full-speed" and "many mirrors have been polished for the preproduction tools." For resists, chemically amplified ones are required to strengthen the relatively weak EUV illumination, but balancing sensitivity, LER, and resolution has proven tricky. The biggest problem is LER, which needs to be <2nm, well below the 4-5nm reported.

Perhaps more than anything, the newest 22nm results should be viewed as a way to "strengthen the confidence of the industry that EUV will become the choice for 22nm and beyond," and thus spur more investments.

Toppan's Kalk: 28nm Tapeouts Proceeding According to Plan

By **Debra Vogler,** Solid State Technology

Toppan Printing has established a new photomask manufacturing process at its photomask facility in Japan, to support 32nm and 28nm semiconductor device production, through an ongoing joint development project with IBM.

CTO at Toppan Photomasks said that 32nm test chips are already being taped out, and by 2H09 and into 1H10, "numerous customers will be ready for production tapeout for 32nm bulk CMOS. Bulk CMOS 28nm test chips for logic are anticipated in 1H10 with bulk production in 2H10.

The fundamental difference from photomasks at 45nm-40nm is the mask material, Kalk explained. "Instead of using molysilicide, we're using an opaque molysilicide over glass [OMOG] at 32nm," a material developed jointly by ShinEtsu and Toppan, now also being used for the 28nm process. It is easier to process than chrome because moly is easier to etch. Chrome requires a chemical etch, with all the attendant issues. Additionally, making molysilicide opaque instead of partially transmitting is a simple adjustment to the oxidation state of the material, a chemistry change in the deposition of the film. OMOG also has extremely good resolution linearity properties, Kalk added.

Toppan's collaboration with IBM began in 2005 at 45nm, and has progressed to the specialized masks to support source mask optimization (SMO) at 22nm. SMO is expected to extend immersion lithography beyond 22nm. Toppan Printing plans to launch volume production of SMO-photomasks in 2011, leveraging the collaboration with IBM.

Kalk's personal belief is that EUV lithography more than likely will not be ready for production until the 16nm logic node, and very few companies will be able to afford it — so double-patterning will be used for the next several years.

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Quarterly technical meetings in the Bay Area
- Reduced registration rates at BACUS Photomask Technology annual meeting
- Eligibility to hold office on BACUS Steering Committee

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Corporate Membership Benefits include:

- One Voting Member in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Exhibit Space discount of 8% at either the Photomask or Advanced Lithography Symposium
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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Calendar

2009

SPIE Photomask Technology

14-17 September
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

SPIE Lithography Asia - Taiwan

18-20 November
Sheraton Taipei Hotel
Taipei, Taiwan
spie.org/la

Abstracts due 2 June 2009

2010

SPIE Advanced Lithography

21-26 February
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
spie.org/al

Abstracts due 10 August 2009

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.

SPIE is an international society advancing light-based technologies.

SPIE
International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 888 504 8171 or +1 360 676 3290
Fax: +1 360 647 1445
customerservice@spie.org • SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE *Europe*
2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 20 89 4747
Fax: +44 29 20 89 4750
spieeurope@spieeurope.org • www.spieeurope.org